LESSON PLAN

Period	Date (Tentative)	Topic	Unit No.	Teaching Methodology	Remarks	Corrective Ac Upon Rev
1	5/10/17	Basic op-Amp Design & Compensation: Genera	I	BB		
		Considerations one-stage op-Amp				
2	6/10/17	Two stage cmos op-Amp, op-Amp gain, freq	II	BB		
3	9/10/17	response - slew rate Symmetric offset	II	BB		
		voltage				
4	10/10	F/B & OP-Amp Compensation - Linear settling	II	BB		
		time,				
5	12/10	op-Amp Compensation	II	BB		
6	13/10	Compensating 2 stage op-Amp	II	BB		
7	13/10	lead Compensation	II	BB		
8	17/10	Compensation independent of	II	BB		
		Process & Temperature				
9	20/10	Current mirrors & Single Stage Amp	II	BB		
10	20/10	Simple, CMOS, BJT Current mirror	II	BB		
11	24/10	Cascade wilson wilder current	II	BB		
		mirrors				

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Period	Date (Tentative)	Topic	Unit No.	Teaching Methodology	Remarks	Corrective Action Upon Review
12	26/10	Common Source	V	PPT		
		Amplifier, Source follower	V			
13	29/10	Common gate Amplifier	V	BB		
14	31/10	Noise : Types of	VI	PPT		
15	2/11	Noise - Thermal Noise	VI	"		
16	5/11	Flicker noise	VI	BB		
17	7/11	Noise in op-Amp's	VI	PPT		
18	9/11	Noise in Common	VI	BB		
19	12/11	Source Stage Noise Bandwidth	VI	BB		
20	14/11	Advanced Current mirrors &	VII	PPT		
		Advanced Current				
21	16/11	mirrors,	VII	BB		
22	19/11	Cascade operational	VII	BB		
23	21/11	Amplifier	VII	BB		

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Period	Date (Tentative)	Topic	Unit No.	Teaching Methodology	Remarks	Corrective Action Upon Review
24	19/11	Current mirror OP-Amp, Linear	III	BB		
		Settling time revisited				
25	21/11	Fully differential OP-Amp	"	PPT		
26	23/11	Common mode F/B ckt,	"	PPT		
27	24/11		"			
28	26/11	Current F/B OP-Amp	"	BB		
		I mid ← 28/11/13 — 2/12/13 →				
29	5/12	PLL: PLL Concepts	IV	BB		
30	7/12	The PLL in the	"	PPT		
31	9/12	Locked Condition	"	PPT		
32	12/12	Integrated ckt PLL's	"	BB		
33	14/12	Phase detector	"	BB		
34	16/12	Voltage Controlled	"	PPT		
35	18/12	Oscillator	"	PPT		

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Period	Date (Tentative)	Topic	Unit No.	Teaching Methodology	Remarks	Corrective Action Upon Review
36		Case Study: Analysis	V	BB		
37	15/12	of the 560 B	"	BB		
		Monolithic PLL	"	BB		
38	19/12	Switched Capacitor circuits: Basic	V	PPT		
	19/12	Building Blocks: op-Amp's, Capacitors	"			
39	21/12	Switches, Non-over laping clocks.	"	BB		
40	22/12	Basic operation & Analysis - resistor	"	BB		
41	22/12	equivalence of Switched Capacitor	"	BB		
42	26/12	Parasitic Sensitive integrator	"	PPT		
43	26/12	Parasitic insensitive integrator	"	PPT		
44	29/12	Signal Flow graph Analysis -	"	PPT		
45	29/12	Filters - Switched fully differential	"	PPT		
		filters, charged injection SC gain				
46	2/01	Parallel res- Cap ckts, Preseliable gain ckt	"	BB		
		Other Switched capacitor ckts				
47	4/01	FWR - Peak detector Sinusoidal Oscillator	"	BB		

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Period	Date (Tentative)	Topic	Unit No.	Teaching Methodology	Remarks	Corrective Action Upon Review
48	5/01/18	Comparators using an op-Amp for	IV	PPT		
		comparator				
49	9/01	charge-injection	"	PPT		
		errors.				
50	11/01	Latched Comparator.	"	PPT		
		Nyquist rate D/A conv				
51	12/01	Decoder Based converter, resistor	"	PPT		
52	12/01	String Converters, Folded resistor	"	PPT		
		String Converter				
53	19/01	Binary scale converters, Binary	"	BB		
54	19/01	weighted resistor converters, Reduced	"	BB		
		resistance ratio ladders.				
55	23/01	R-2R Based Converters, ~~Thermometer~~ ~~Seg. converters~~, code	"	PPT		
		current mode D/A converters.				
56	25/01	Nyquist rate A/D conver. Integrating Converters	"	PPT		
		SAR converters.				
57	26/01	DAC Based SAR, Flash converters.	"	PPT		
58	26/01	Time interleaved A/D converters.	"	PPT		