BB: Black Board.

LESSON PLAN

Period	Date (Tentative)	Topic	Unit No.	Teaching Methodology	Remarks	Corrective Action Upon Review
1	5/10/17	Historical perspective	I	BB		
2	5/10/17	Issues in DICD	I	BB		
3	9/10/17	Quality Metrics	I	BB		
4	9/10/17	cost of an IC	I	BB		
5	12/10/17	Functionality	I	BB		
6	12/10/17	Robustness	I	BB		
7	16/10/17	performance	I	BB		
8	16/10/17	power of IC	I	BB		
9	23/10/17	Energy consumption	I	BB		
10	23/10/17	The MOS Transistor	II	BB		

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11	26/10/17	N-MOS P-MOS operation	II	BB		
12	26/10/17	Static conditions	II	BB		
13	30/10/17	Dynamic Behaviour	II	BB		
14	30/10/17	The actual MOS transistor	II	BB		
15	2/11/17	Secondary effects	II	BB		
16	2/11/17	Spice Models for MOS	II			
17	6/11/17	Method of Logical effort for Transistor sit	II	BB		
18	6/11/17	Transistor sizing	II	BB		
19	9/11/17	CMOS Inverter basics	III	BB		
20	9/11/17	Intitutive perspective	III	BB		
21	13/11/17	Evaluation	III	BB		
22	13/11/17	performance	III	BB		

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23	16/11/17	Static Behaviour	III			
24	16/11/17	Dynamic Behaviour	III			
25	20/11/17	Switching Threshold	III			
26	20/11/17	Noise Margins	III			
27	23/11/17	Robustness, performance, Dynamic Behaviour	III			
28	23/11/17	Computing capacitances	III			
29	4/12/17	CMOS logic family	IV	BB		
30	4/12/17	TTL	IV	BB		
31	7/12/17	ECL	IV	BB		
32	7/12/17	CMOS/TTL	IV	BB		

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Period	Date (Tentative)	Topic	Unit No.	Teaching Methodology	Remarks	Corrective Action Upon Review
33	11/12/17	Interfacing of Logic families, Comparison	IV	BB		
34	11/12/17	VHDL-DECODER	IV	BB		
35	14/12/17	VHDL ENCODER, VHDL MUX	IV	BB		
36	14/12/17	ADDERS/Subtractor	IV	BB		
37	18/12/17	VHDL LATCHES/FLIPS	IV	BB		
38	18/12/17	VHDL-SR,JK FLIPFLOPS	V	BB		
39	21/12/17	VHDL-D,T FLIPFLOPS	V	BB		
40	21/12/17	VHDL-COUNTERS, SHIFT REGISTERS	V	BB		
41	28/12/17	ASM-VHDL	V	BB		
42	28/12/17	PIS-MUX, DECODERS	V	BB		

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43	1/1/18	DECODERS BARREL SHIFTER COUNTERS	V	BB		
44	1/1/18	Digital single bit adder	V	BB		
45	4/1/18	MEMORIES: ROM internal structure	VI	BB		
46	4/1/18	2D - DECODING TIMING, APPLICATIONS	VI	BB		
47	8/1/18	RAM-Internal structure	VI	BB		
48	18/1/18	CPLD XC9500 Series, architecture	VI	BB		
49	18/1/18	CLB, I/O BLOCK Internal structure	VI	BB		
50	22/1/18	FPGA: Conceptual view	VI	BB		
51	25/1/18	CLB classification Internal architecture	VI	BB		
52	25/1/18	FP block architecture	VI	BB		