LESSON PLAN

Subject Code & Name: Digital System Design & Techniques

Branch: VLSI Class / Semester: IM.Tech-SEM 1 Academic Year:2017-18
Faculty: J.Swathi

Period	Date (Tentative)	Topic	Unit No.	Teaching Methodology	Remarks	Corrective action upon review
		DESIGN OF DIGITAL SYSTEMS	**I**			
1	05/10/17	Introduction		BB		
2	05/10/17	ASM charts		BB		
3	10/10/17	Data path design		BB		
4	10/10/17	Control logic implementation		BB		
5	12/10/17	Equivalent states and state tables		BB		
6	12/10/17	Reduction of state tables- Row matching method		BB		
7	17/10/17	Reduction of state tables- Implication chart method		BB		
8	17/10/17	Equivalent state assignments		BB		
9	24/10/17	Derivation Flipflop input equations		BB		
10	24/10/17	Guide lines for state assignments		BB		
		SEQUENTIAL CIRCUIT DESIGN	**II**			
11	26/10/17	Design of iterative circuits		BB		
12	26/10/17	Introduction to ROM & PLA		BB		
13	31/10/17	Design of sequential circuits using ROM		BB		
14	31/10/17	Design of sequential circuits using PLA		BB		
15	02/11/17	Introduction to FPGA &CPLD		BB		
16	02/11/17	Design of sequential circuits using FPGA		BB		
17	07/11/17	Design of sequential circuits using CPLD		BB		
		FAULT MODELING	**III**			
18	07/11/17	Fault classes and models		BB		
19	09/11/17	Stuck at faults, Bridging faults		BB		
20	09/11/17	Transition and Intermittent faults		BB		
21	14/11/17	Test Generation		BB		
22	14/11/17	Fault diagnosis of combinational circuits		BB		
23	16/11/17	Fault table method		BB		
24	16/11/17	Path sensitization Algorithm		BB		
25	21/11/17	Boolean difference method		BB		
26	21/11/17	Kohavi Algorithm		BB		
		TEST PATTERN GENERATION	**IV**			

27	23/11/17	D-Alogorithm		BB		
28	23/11/17	PODEM		BB		
29	05/12/17	Random testing		BB		
30	05/12/17	Transition count testing		BB		
32	07/12/17	Signature analysis		BB		
33	07/12/17	Testing for bridging faults		BB		
34	12/12/17	Fault diagnosis in sequential circuits		BB		
35	12/12/17	State identificationc experiments – successor tree		BB		
36	14/12/17	Homing,synchronizing experiments		BB		
37	14/12/17	distinguishing experiments		BB		
38	19/12/17	Machine identification experiments		BB		
39	19/12/17	Fault detection experiments		BB		
		PROGRAMMING LOGIC ARRAYS	**V**			
40	21/12/17	Introduction to PLA		BB		
41	21/12/17	Design using PLA		BB		
42	26/12/17	PLA Minimization		BB		
43	26/12/17	PLA Folding-Row & column folding		BB		
44	28/12/17	PLA Testing		BB		
45	28/12/17	Fault models in PLA		BB		
46	09/01/18	Test generation for PLA		BB		
47	09/01/18	Testable PLA design		BB		
		ASYNCHRONOUS SEQUENTIAL MACHINE	**VI**			
48	11/01/18	Fundamental mode model		BB		
49	11/01/18	Flow table		BB		
50	18/01/18	State reduction		BB		
51	18/01/18	Minimal closed covers,Races		BB		
52	23/01/18	Cycles,hazards		BB		

CR: CLASS ROOM **PPT: POWER POINT PRESENTATION** **LCD**

TEXT BOOKS:

1. Z. Kohavi – "Switching & finite Automata Theory" (TMH).
2. N. N. Biswas – "Logic Design Theory" (PHI).
3. Nolman Balabanian, Bradley Calson – "Digital Logic Design Principles" – Wily Student Edition 2004.

REFRENCE BOOKS:

1. M. Abramovici, M. A. Breues, A. D. Friedman – "Digital System Testing and Testable Design", Jaico Publications.
2. Charles H. Roth Jr. – "Fundamentals of Logic Design".
3. Frederick. J. Hill & Peterson – "Computer Aided Logic Design" – Wiley 4th Edition.

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